

EAST - [10694990.wsp:1]

File View Edit Tools Window Help

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L1: (141574) charge near coupled near devices or CCD or CMOS near image\$1 near device or image ne...
 L3: (40617) CMOS near image\$1 near device or image near device
 L4: (188) 3 and trench\$2 and dop\$3
 L5: (258) 3 and trench\$2
 L6: (40) 5 and (trench\$2 with dop\$3)
 L7: (1) ("6794698").PN.
 L8: (1) ("6624016").PN.
 L9: (1) ("6417074").PN.
 L10: (1) ("6069058").PN.
 L11: (1) ("5943589").PN.
 L2: (586) 1 and trench\$2 and dop\$1

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 DB: US-PGPUB:USPAT:EP ☐ Flush
 Default operator: OR ☒ Highlight all hits immediately
 5 and (trench\$2 with dop\$3)

BR5 form IS&S form Image Text HTML

	U	I	Document ID	Issue Date	Pages	Title	Current OR	Current XRef
1	<input type="checkbox"/>	<input type="checkbox"/>	US 20050045926 A1	20050303	19	Suppression of dark current in a photosensor for imaging	257/291	
2	<input type="checkbox"/>	<input type="checkbox"/>	US 20050042793 A1	20050224	14	Reduced barrier photodiode/gate device structure for high efficiency charge transfer and reduced lag and method of formation	438/57	
3	<input type="checkbox"/>	<input type="checkbox"/>	US 20050035382 A1	20050217	24	Solid state image sensing device having pixels provided with barrier layer underneath transistor regions and camera using said device	257/290	
4	<input type="checkbox"/>	<input type="checkbox"/>	US 20040262646 A1	20041230	16	Pixel design to maximize photodiode capacitance and method of forming same	257/233	438/45
5	<input type="checkbox"/>	<input type="checkbox"/>	US 20040262609 A1	20041230	16	REDUCED BARRIER PHOTODIODE/TRANSFER GATE DEVICE STRUCTURE OF HIGH EFFICIENCY CHARGE TRANSFER AND REDUCED LAG AND METHOD OF FORMATION	257/72	
6	<input type="checkbox"/>	<input type="checkbox"/>	US 20040253761 A1	20041216	16	Well for CMOS imager and method of formation	438/84	
7	<input type="checkbox"/>	<input type="checkbox"/>	US 20040251481 A1	20041216	34	Isolation region implant permitting improved photodiode structure	257/292	
8	<input type="checkbox"/>	<input type="checkbox"/>	US 20040235216 A1	20041125	19	Multi-trench region for accumulation of photo-generated charge in a CMOS imager	438/60	
9	<input type="checkbox"/>	<input type="checkbox"/>	US 20040195600 A1	20041007	20	Trench photosensor for a CMOS imager	257/292	
10	<input type="checkbox"/>	<input type="checkbox"/>	US 20040195592 A1	20041007	12	Two-transistor pixel with buried reset channel and method of formation	257/202	
11	<input type="checkbox"/>	<input type="checkbox"/>	US 20040183771 A1	20040930	13	Salicided MOS device and one-sided salicided MOS device, and simultaneous fabrication method therefor	257/382	257/383; 257/389; 438/300